Amendments to the Claims

Please amend the claims as follows:

1. (Currently Amended) An information processing apparatus to which a memory cartridge having a program memory is attached, comprising:

a system bus which is connected to said program memory upon attaching said memory cartridge;

a processor ~~which is~~ connected to said system bus ~~and processes~~ for processing a program stored in said program memory and for generating a pulse signal;

a power control circuit coupled to said processor for supplying power to said information processing apparatus when said pulse signal is generated;

a detecting means ~~which detects~~ for detecting an error of said processor; and

a stopping means for ~~shutting down~~ stopping the power control circuit from supplying the power to said information processing apparatus when the detecting means detects the error of said processor and when said processor stops generating said pulse signal, wherein said information processing apparatus goes into an off-state without depending on a timer ~~further searching another processor~~ ~~when said error is detected~~.

2. (Currently Amended) An information processing apparatus according to claim 1, wherein said processor generates [[a]] said pulse signal on the basis of said program,

said detecting means includes a charging and discharging means which repeats a charge and discharge in response to said pulse signal, and

said stopping means stops said power supply when a charged voltage of said charging and discharging means does not meet a predetermined condition.

3. (Previously Presented) An information processing apparatus according to claim 2, wherein said pulse signal is a signal having a level that varies between the low-level and the high-level periodically,

said charging and discharging means includes a first capacitor which discharges an electric charge when said pulse signal is said low-level, and charges an electric charge when said pulse signal is said high-level, and a second capacitor which charges an electric charge when said pulse signal is said low-level, and discharges an electric charge when said pulse signal is said high-level, and

said stopping means stops said power supply when a charged voltage of at least one of said first capacitor and said second capacitor exceeds a predetermined value.

4. (Previously Presented) An information processing apparatus according to claim 2 or 3, further comprising:

an instructing means which instructs a reset of said processor; and

a discharging path which is enabled in response to an instruction of said instructing means and discharges an electric charge being charged in said charging and discharging means.

5. (Original) A memory cartridge system, comprising:

a memory cartridge having a program memory;

a processor which is connected to said program memory upon attaching said memory cartridge and processes a program stored in said program memory;

a capacitor which is repeatedly charged and discharged in response to a pulse signal; and

a stopping means which stops a power supply to said processor when a charged voltage of said capacitor does not meet a predetermined condition,

wherein said program includes a level control program which maintains the charged voltage of said capacitor within a predetermined condition by varying a level of said pulse signal in each predetermined period.

6. (Original) A memory cartridge which is detachably attached to an information processing apparatus which stops a power supply to a processor when a charged voltage of a capacitor does not meet a predetermined condition, and stores a program which allows said processor to execute, wherein

said program includes a capacitor control program which maintains the charged voltage of said capacitor within said predetermined condition by charging and discharging said capacitor in each predetermined period.

7. (Currently Amended) A home-use game device, comprising:

a system bus which is connected to a program memory upon attaching a memory cartridge having a program memory;

a processor ~~which is~~ connected to said system bus ~~and processes~~ for processing a game program stored in said program memory and for generating a pulse signal;

a power control unit coupled to said processor for supplying power to said home-use game device when said pulse signal is generated;

a detecting means ~~which detects~~ for detecting an error of said processor; and

a stopping means for ~~shutting down~~ stopping the power control unit from supplying the power to said home-use game device when the detecting means detects the error of said processor and when said processor stops generating said pulse signal, wherein said home-use game device goes into an off-state without depending on a timer ~~further searching another processor when said error is detected~~.

8. (Currently Amended) A home-use karaoke device, comprising:

a system bus which is connected to a program memory upon attaching a memory cartridge having a program memory;

a processor ~~which is~~ connected to said system bus ~~and processes~~ for processing a karaoke program stored in said program memory and for generating a pulse signal;

a power control unit coupled to said processor for supplying power to said home-use karaoke device when said pulse signal is generated;

a detecting means ~~which detects~~ for detecting an error of said processor; and

a stopping means for ~~shutting down~~ stopping the power control unit from supplying the power to said home-use karaoke device when the detecting means detects the error of said processor and when said processor stops generating said pulse signal, wherein said home-use karaoke device goes into an off-state without depending on a timer ~~further searching another processor when said error is detected~~.

9. (Previously Presented) A home-use game device, comprising:

a system bus which is connected to a program memory upon attaching a memory cartridge having a program memory;

a processor which is connected to said system bus and processes a game program stored in said program memory;

a detecting means which detects an error of said processor; and

a stopping means which stops a power supply to said processor when said error is detected,

wherein said processor generates a pulse signal on the basis of said program,

said detecting means includes a charging and discharging means which repeats a charge and discharge in response to said pulse signal, and

said stopping means stops said power supply when a charged voltage of said charging and discharging means does not meet a predetermined condition.

10. (Previously Presented) A home-use karaoke device, comprising:

a system bus which is connected to a program memory upon attaching a memory cartridge having a program memory;

a processor which is connected to said system bus and processes a karaoke program stored in said program memory;

a detecting means which detects an error of said processor; and

a stopping means which stops a power supply when said error is detected,

wherein said processor generates a pulse signal on the basis of said program,

said detecting means includes a charging and discharging means which repeats a charge and discharge in response to said pulse signal, and

said stopping means stops said power supply when a charged voltage of said charging and discharging means does not meet a predetermined condition.

11. (Previously Presented) An information processing apparatus to which a memory cartridge having a program memory is attached, comprising:

a system bus which is connected to said program memory upon attaching said memory cartridge;

a processor which is connected to said system bus and processes a program stored in said program memory;

a detecting means which detects an error of said processor; and

a stopping means for shutting down said information processing apparatus into an off-state when said error is detected,

wherein said processor generates a pulse signal on the basis of said program,

said detecting means includes a charging and discharging means which repeats a charge and discharge in response to said pulse signal, and

said stopping means stops said power supply when a charged voltage of said charging and discharging means does not meet a predetermined condition.

12. (Previously Presented) A home-use game device, comprising:

a system bus which is connected to a program memory upon attaching a memory cartridge having a program memory;

a processor which is connected to said system bus and processes a game program stored in said program memory;

a detecting means which detects an error of said processor; and

a stopping means for shutting down said game device into an off-state when said error is detected,

wherein said processor generates a pulse signal on the basis of said program,

said detecting means includes a charging and discharging means which repeats a charge and discharge in response to said pulse signal, and

said stopping means stops said power supply when a charged voltage of said charging and discharging means does not meet a predetermined condition.

13. (Previously Presented) A home-use karaoke device, comprising:

a system bus which is connected to a program memory upon attaching a memory cartridge having a program memory;

a processor which is connected to said system bus and processes a karaoke program stored in said program memory;

a detecting means which detects an error of said processor; and

a stopping means for shutting down said karaoke device into an off-state when said error is detected,

wherein said processor generates a pulse signal on the basis of said program,

said detecting means includes a charging and discharging means which repeats a charge and discharge in response to said pulse signal, and

said stopping means stops said power supply when a charged voltage of said charging and discharging means does not meet a predetermined condition.

14. (Previously Presented) An information processing apparatus according to claim 11, wherein said pulse signal is a signal having a level that varies between the low-level and the high-level periodically,

said charging and discharging means includes a first capacitor which discharges an electric charge when said pulse signal is said low-level, and charges an electric charge when said pulse signal is said high-level, and a second capacitor which charges an electric charge when said pulse signal is said low-level, and discharges an electric charge when said pulse signal is said high-level, and

said stopping means stops said power supply when a charged voltage of at least one of said first capacitor and said second capacitor exceeds a predetermined value.

15. (Previously Presented) An information processing apparatus according to claim 14, further comprising:

an instructing means which instructs a reset of said processor; and

a discharging path which is enabled in response to an instruction of said instructing means and discharges an electric charge being charged in said charging and discharging means.